

What is claimed is:

1        1.    A method, comprising:  
2        forming a trench in a semiconductor substrate surface;  
3        depositing a dielectric material onto the  
4 semiconductor substrate surface and into the trench;  
5        implanting ions into at least some of the dielectric  
6 material to form an implanted dielectric region; and  
7        polishing the semiconductor substrate surface to  
8 remove at least some of the implanted dielectric region.

1        2.    The method of claim 1, wherein forming the trench  
2 comprises forming a barrier layer on the semiconductor  
3 substrate surface.

1        3.    The method of claim 2, further comprising  
2 implanting ions into at least some of the barrier layer.

1        4.    The method of claim 2, wherein implanting ions  
2 comprises implanting ions at least as deep as the barrier  
3 layer.

1        5.    The method of claim 1, wherein the semiconductor  
2 substrate is a silicon wafer, and forming the trench  
3 comprises patterning a mask layer on a surface of the  
4 silicon wafer such that at least one region of the surface  
5 is exposed, and etching the trench in the exposed region.

1           6.    The method of claim 1, wherein implanting ions  
2 comprises implanting silicon.

1           7.    The method of claim 1, wherein implanting ions  
2 comprises implanting carbon.

1           8.    The method of claim 1, wherein implanting ions  
2 comprises implanting oxygen.

1           9.    The method of claim 1, wherein implanting ions  
2 comprises implanting nitrogen.

1           10.   A method, comprising:  
2           forming a nitride layer on a silicon wafer surface,  
3 the nitride layer having a first polish rate;  
4           etching a plurality of recesses in the silicon wafer  
5 surface;  
6           forming an oxide layer on the silicon wafer surface  
7 and in the plurality of recesses, the oxide layer having a  
8 second polish rate;  
9           implanting ions into at least one of the nitride layer  
10 and the oxide layer to form an implanted region having a  
11 third polish rate different from the first and second  
12 polish rates; and

13        polishing the silicon wafer surface to remove at least  
14        some of the oxide layer and at least some of the implanted  
15        region therefrom.

1        11. The method of claim 10, wherein polishing  
2        comprises removing at least some of the nitride layer.

1        12. The method of claim 10, wherein polishing  
2        comprises chemical mechanical polishing.

1        13. The method of claim 10, wherein the ions are  
2        selected from the group consisting of silicon, carbon,  
3        nitrogen, and oxygen.

1        14. The method of claim 10, wherein implanting ions  
2        changes one of the first and second polish rates relative  
3        to the other polish rate.

1        15. An apparatus comprising:  
2        a semiconductor substrate having a barrier layer  
3        formed thereon;  
4        a trench etched into the substrate adjacent the  
5        barrier layer;  
6        a dielectric layer deposited over the barrier layer  
7        and trench; and

8           a plurality of ions implanted into the dielectric  
9 layer.

1           16. The apparatus of claim 14 further comprising a  
2 plurality of ions implanted into the barrier layer.

1           17. The apparatus of claim 14 wherein the barrier  
2 layer comprises a silicon nitride layer.

1           18. The apparatus of claim 14 wherein the dielectric  
2 layer comprises a silicon oxide layer.

1           19. The apparatus of claim 14 wherein the dielectric  
2 layer is damaged by the plurality of implanted ions.

1           20. The apparatus of claim 14 wherein the plurality  
2 of ions are selected from the group consisting of silicon,  
3 carbon, nitrogen, and oxygen.